CLAIMS

1. (Currently Amended) A processor comprising:

a cache having a plurality of hit lines; and

a selector to provide a data during a clock cycle from a plurality of memory locations associated with the plurality of hit lines in the cache;

a multi-hit detection circuit coupled to the hit lines to detect multiple hits in the cache during the clock cycle based on hit signals on the hit lines, the multi-hit detection circuit comprising a NAND gate ~~with~~ having pull-down transistor pairs coupled to the hit lines to pull an output node of the NAND gate low if two different hit signals include a hit; and

an error flag generated by an inverter output coupled to the output node of the NAND gate in the multi-hit detection circuit during the clock cycle, the error flag to indicate that the data provided during the clock cycle is invalid if multiple cache hits are detected, the error flag to indicate that the data provided during the clock cycle is valid if a single cache hit is detected.

2. (Original) The processor of claim 1, wherein the cache includes a plurality of comparators coupled to the hit lines to generate the hit signals based on comparisons between cache tags and a lookup tag.

3. (Original) The processor of claim 2, wherein the selector includes a multiplexer coupled to the hit lines to select data based on the hit signals.

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Original) The processor of claim 5, wherein the cache is a multi-way set associative cache.

8. - 12. (Cancelled)

13. (Currently Amended) A method of detecting multi-hit errors in a cache, the method comprising:

comparing a plurality of cache tags stored in each of a plurality of ways associated with a indexed set to a lookup tag to generate a plurality of hit signals during a clock cycle;

selecting selected data from a plurality of memory locations associated with the indexed set based on the plurality of hit signals during the clock cycle;

comparing pairs of the plurality of hit signals during the clock cycle using a NAND gate with transistor pairs to determine if any two hit signals both indicate a multiple cache hit;

generating an error flag using an inverter output during the clock cycle to indicate the invalidity of the selected data if the multiple hit is detected; and

generating the error flag to indicate the validity of the selected data if the multiple cache hit is not detected, wherein the plurality of hit signals are paired to gates of series-coupled pull-

down transistor pairs of a NAND gate and an output of the NAND gate is inverted to generate the error flag.

14. (Previously Presented) The method of claim 13, wherein comparing the plurality of cache tags includes comparing four cache tags of a four-way set associative cache to the lookup tag to generate four hit signals.

15. (Original) The method of claim 14, wherein generating the error flag includes providing all pairings of the plurality of hit signals to gates of series-coupled pull-down transistor pairs of a NAND gate.

16. (Cancelled)

17. (Cancelled)